Loren Ashfield

Computer Engineer at UCSB, 3.93 GPA

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About

I am a rising senior computer engineering student at UCSB. I am passionate about computers and interested in pursuing opportunities in VLSI design and computer architecture. I am proficient with a range of industry standard design, simulation, and verification tools, including Cadence, SPICE, Verilog, and others. I am also experienced in developing full-stack, end-to-end software. Additionally, I have hands-on experience with applying novel AI and machine learning models to industrial applications. I excel at approching problems with an innovative and analytical mindset, backed by a strong intution, dedicatied work ethic, and vivid eagerness to learn. Most importantly, I thrive in team-based environments, emphasizing communication in my work.

Education

UC Santa Barbara		Santa Barbara, CA	
BS, Computer Engineering		2022 - 2026	
Newark Academy		Livingston, NJ	
High School Diploma		2018 - 2022	
Experience			
ECE Tutor	UC Santa Barbara	02/2025 - Present	
• Working for MESA University Program at income students.	UCSB providing one on one tutoring for	first-generation and low-	
• Tutoring Digital Design Principles (ECE 1524	A)		
Lab Systems Engineer	Yonder Materials	08/2024 - Present	
• Creating full-stack software applications to power AI-driven, high-throughput materials discovery.			
• Working in lab alongside chemistry team, engaging hands on with deliverables and shadowing experienced material researchers.			
$^{\circ}$ Designing custom circuits to allow software to work fluidly with high-throughput electrochemistry setup.			
Embedded Systems Research Assistant	Universidad Carlos III de Madrid	06/2024 - 07/2024	
• Evaluated the effects of random bit changes Space applications.	on consumer grade microprocessors to de	etermine reliability in New	
• Wrote low footprint benchmarks for ARM Cortex-M and RISC-V embedded processors using explicit register management, testing with and without operating systems.			
• Prepared the benchmark for irradiation ca communication to catalog misbehaviors.	mpaigns controlled by an external host,	sending data over serial	
Computer Repair	Freelance	01/2020 - 06/2022	
• Provided practical repairs for personal comp clients through issues and advising cost-effect	uter devices and peripherals. Performed or tive solutions.	n-site repairs while talking	
• Gained a practical intuition for working with	circuits and working directly with clients.		
Various Summer Jobs	Corolla, NC	2021 - 2023	
Held jobs in the service industry during highWorked in the kitchen, as a food runner, and	school, learning customer service and con at the counter.	nmunication.	
Projects			

ULTRARAM/2D Integration

• Exploring the possibility of fabricating ULTRARAM, a novel memory concept built on III-V materials, on wafers utilizing 2D material substrates.

Present

32kb SRAM

- $\circ~$ Designed 32kb SRAM from scratch on Cadence Virtuoso on a 130nm process node.
- $\circ~$ Built all necessary circuits to power SRAM array, including precharge circuitry, sense amps, decoders, and more.
- $\circ~$ Ran SPICE tests to verify and benchmark SRAM performance, corroborated by hand calculations.

Societies and Honors

Dean's Honors, UCSB, Earned every quarter since matriculation	2022 - 2024
Tau Beta Pi, Member of national engineering honor society	2024
Alpha Tau Omega, Social Chair, coordinated large scale trips and events for social fraternity	2024

Skills

Programming Languages: Python, C/C++, Assembly, Java

Tools and Frameworks: Cadence, LTspice, ModelSim, Quartus, SUE Design Manager, NST (New SPICE Tool), Git, Verilog, SystemVerilog, VHDL, Conda, PyTorch, Linux, Streamlit, PyQT, Docker, Poetry **Languages:** English